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EXAMINER	
FLORES, LEON	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,730	SONI ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-20) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that *"Miller does not teach nor otherwise suggest accessing the ROM values during processing of data samples. On the contrary, the Miller disclosure is directed at adjusting various parameters of a delay line based on a given communication protocol, prior to communication, i.e. prior to processing of data samples, based on said communication protocol".*

The examiner respectfully disagrees. The reference of Miller does teach a ROM that contains, at various addresses, the control signals used to adjust/control the rate and the length of the delay line. By simply changing from one address to another, the demodulator may be made to operate under different protocols. (See col. 4, line 58 - col. 5, line 1) Furthermore, Miller also discloses a delay line for storing samples, means for shifting successive samples through said delay line, means for determining the effective length of said delay line, and a control circuit for activating said means (rate and length) for selecting the rate and length at which samples are shifted through said delay line. (See claim 1)

Applicant further asserts that *"the Miller CLOCK SELECT signal is substantially distinct from a signal of completion of a processing event".*

The examiner respectfully disagrees. The reference of Miller teaches a mode control circuit for selecting/adjusting the rate and length at which samples are shifted through the delay line. The selection of the CLOCK SELECT is dependent on a mode select. The mode select is process by a processing device called ROM.

Applicant further asserts that *"within the Miller system implementation, the Miller CLOCK SELECT signal is disclosed as a single value signal fed directly to the Miller delay line 20 (see Figs. 1 and 3); therefore, it cannot determine two shift data rates, i.e. a higher output rate than an input rate, as recited in claim 1".*

The examiner respectfully disagrees. The clock select signal adjusts the rate at which samples are shifted through the delay line. One skilled in the art would know that when the rate of the delay line is increased the output rate is greater than the rate at which the samples are inputted into the delay.

Applicant further asserts that *"within the Miller system implementation, the Miller CLOCK SELECT signal controls the shift rate through the delay line 20 according to a selected communication protocol and cannot trigger a reduction of the delay line 20 in response to its detection. The Miller CLOCK SELECT signal is permanently fed to the Miller delay line and has a fixed value in operation, associated with the selected communication protocol".*

The examiner respectfully disagrees. The reference of Miller does teach that the control signals may be fully static signals. (See col. 4, lines 58-61)

Applicant further asserts that *"it would not have been obvious to one of ordinary skill in the art to incorporate the CLOCK SELECT feature into the system of Miller and*

obtain the step of in response to receiving a signal of completion of a processing event, reducing the length of the delay chain by shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming into the delay chain, as claimed in claim 1".

The examiner respectfully disagrees. Please see rejection of claim 1. However, taking the contrary, a new ground of rejection has been issued wherein the reference of Warren, which applicant is silent, is used to reject claim 1. Furthermore, this new ground of rejection does substitute, in any way, the previous rejection.

Applicant finally asserts that *"the CLOCK SELECT control signal, the Miller DELAY SELECT control signal is also provided via ROM (see Fig. 1 and col 4, lines 19-26 and 58-68) and its value is fixed once a communication protocol is selected. Therefore the length of the Miller delay line 20 is also fixed during communication and does not change or get reduced dynamically as data samples continue to be read into the delay line".*

The examiner respectfully disagrees. The reference of Miller does teach that the control signals may be fully static signals. (See col. 4, lines 58-61)

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. **Claims (1, 14-15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434)**

Re claim 1, Miller discloses a method of digitally processing a sequence of data samples comprising: reading the sequence of data samples into a tapped clocked delay chain (See fig. 1: the input to element 20); processing data samples from taps on the clocked delay chain. (See fig. 1: 20)

But the reference of Miller fails to explicitly teach that in response to receiving a signal of completion of a processing event, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain.

However, the reference of Miller does suggest the teaching of mode control

which, in response to determining a clock select, determines the speed with which the signal moves through the delay line. (See fig. 1: 26 "CLOCK SELECT" & col. 1, lines 54-56 & col. 4, lines 24-26 & col. 4, line 58 – col. 5, line 1 & claim 1)

Therefore, it would have been obvious (obvious to try) to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed, for the benefit of selecting the rate which samples are shifted through the delay line.

The reference of Miller discloses the limitations as claimed above, except he fails to explicitly teach dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain.

However, the reference of Miller does suggest the teaching of mode control which, in response to determining a delay select, determines the length of delay line. (See fig. 1: 26 "DELAY SELECT" & col. 1, lines 67-68 & col. 4, lines 22-24 & col. 4, line 58 – col. 5, line 1 & claim 1)

Therefore, it would have been obvious (obvious to try) to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed, for the benefit of determining and reducing the length of the delay line.

Claim 14 is an apparatus claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in apparatus claim 14. Therefore, claim 14 has been analyzed w/r to claim 1 above.

Claim 15 has been analyzed and rejected w/r to claim 1 above.

2. **Claims (2-3, 10-11) are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434), as applied to claim 1 above, and further in view of Applicant Admitted Prior Art. (hereinafter Prior art)**

Re claim 2, the reference of Miller fails to explicitly teach that wherein the data samples are from a data packet.

However, Prior art does. (See page 1, line 20 – page 2, line 10) Prior art discloses that, during timing acquisition of a 802.11a packet, samples are often tapped from registers in a delay chain.

Therefore, taking the combined teachings of Miller and Prior art as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed and as taught by Prior art, for the benefit of complying with IEEE standards.

Re claim 3, the combination of Miller and Prior art further discloses that wherein the data packet conforms to a transmission system selected from the group of 802.11 a, 802.11 g and HIPERLAN/2 transmission systems. (In Prior art, see page 1, line 20 – page 2, line 10)

Claim 10 has been analyzed and rejected w/r to claim 2 above.

Claim 11 has been analyzed and rejected w/r to claim 3 above.

3. **Claims (4-5) are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434), as applied to claim 1 above, and further in view of Warren et al. (hereinafter Warren) (US Patent 6,075,807)**

Re claim 4, the reference of Miller fails to explicitly teach that wherein the event includes a synchronization of the data packet.

However, Warren does. (See fig. 1 & col. 4, lines 24-39) Warren discloses that after synchronization has been achieved, the bit synchronization logic unit may adjust the propagation rate of the delay line.

Therefore, taking the combined teachings of Miller and Warren as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed and as taught by Warren, for the benefit of achieving synchronization.

Re claim 5, the combination of Miller and Warren further discloses that wherein the clocked delay chain comprises a plurality of pipelined registers. (In Warren, see col. 3, lines 42-44)

4. **Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434) and Warren et al. (hereinafter Warren) (US Patent 6,075,807)**

Re claim 6, the combination of Miller and Warren fail to explicitly teach that wherein the reducing the length of the clocked delay chain is performed until a desired

length of the clocked delay chain is achieved.

However, the reference of Miller does suggest the teaching of mode control which, in response to determining a delay select, determines the length of delay line. (See fig. 1: 26 "DELAY SELECT" & col. 1, lines 67-68 & col. 4, lines 22-24)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Miller, as modified by Warren, in the manner as claimed, for the benefit of determining and reducing the length of the delay line.

5. **Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434) and Warren et al. (hereinafter Warren) (US Patent 6,075,807)**

Re claim 7, the combination of Miller and Warren fail to explicitly teach that wherein reducing the length of the clocked delay chain further includes bypassing empty registers.

However, the reference of Miller does suggest the teaching of mode control which, in response to determining a delay select, determines the length of delay line. (See fig. 1: 26 "DELAY SELECT" & col. 1, lines 67-68 & col. 4, lines 22-24) Furthermore, one skilled in the art would know that if the length of delay line is reduced some of the registers in the delay line will be bypassed.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Miller, as modified by Warren, in the manner as claimed, for the benefit of determining and reducing the length of the delay line.

6. **Claims (8 & 13) are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434) and Warren et al. (hereinafter Warren) (US Patent 6,075,807)**

Re claim 8, Warren discloses a method of digitally processing a sequence of data samples of a data packet comprising: reading the sequence of data samples from a data packet into a tapped clocked delay chain comprising a plurality of pipelined registers (See fig. 1 & col. 3, lines 42-44); processing data samples from taps on the clocked delay chain to synchronize a data packet. (See fig. 1 & col. 4, lines 19-40)

But the reference of Warren fails to explicitly teach that in response to receiving a signal of completion of synchronization of the data packet, shifting samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain.

However, the reference of Warren does suggest the teaching of adjusting the propagation rate of the delay line once synchronization has been achieved. (See fig. 1 & col. 4, lines 24-39)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Warren, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Warren discloses the limitation as claimed above, except he fails to explicitly teach reducing the length of the clocked delay chain by bypassing empty registers as data samples continue to be read into the clocked delay chain; and repeating the steps of shifting data samples rapidly out of the clocked delay chain at a

higher output rate than the input rate and reducing the length of the clocked delay chain.

However, Miller does. (See fig. 1: 26 "DELAY SELECT" & col. 1, lines 67-68 & col. 4, lines 22-24) Miller discloses mode control which, in response to determining a delay select, determines the length of delay line. The reference of Miller further teaches signals L0 to L7, which are the 8 bits of the DELAY SELECT control signal. These bits determine the length of the delay line by short circuiting or bypassing shift registers. (See fig. 3 & col. 5, lines 52-60) Furthermore, in response to determining a clock select, determines the speed with which the signal moves through the delay line. (See fig. 1: 26 "CLOCK SELECT" & col. 1, lines 54-56 & col. 4, lines 24-26)

Therefore, taking the combined teachings of Warren and Miller as a whole, it would have been obvious (obvious to try) to one of ordinary skills in the art to incorporate this feature into the system of Warren, in the manner as claimed and as taught by Miller, for the benefit of controlling the length of the delay line.

Claim 13 is an apparatus claim corresponding to method claim 8. Hence, the steps performed in method claim 8 would have necessitated the elements in apparatus claim 13. Therefore, claim 13 has been analyzed w/r to claim 8 above.

7. **Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434)**

Re claim 9, Miller discloses an apparatus comprising: a pipeline of registers that store data samples (See fig. 3 & col. 5, lines 24-25); logic circuitry which controls each

individual register of the pipeline of registers (See fig. 3: 44); a multiplexer having inputs from select registers from the pipeline of registers, and an output. (See fig. 3 & col. 5, lines 25-26)

But the reference of Miller fails to explicitly teach that a processor which controls the data shifting rates, the logic circuitry, and the output of the multiplexer based on a plurality of processing events of the apparatus.

However, the reference of Miller does suggest the teaching of mode control which, in response to determining a clock select, determines the speed with which the signal moves through the delay line. (See fig. 1: 26 "CLOCK SELECT" & col. 1, lines 54-56 & col. 4, lines 24-26)

Therefore, it would have been obvious (obvious to try)to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed, for the benefit of selecting the rate which samples are shifted through the delay line.

8. **Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434)**

Re claim 16, the reference of Miller fails to explicitly teach bypassing an empty portion of clocked delay chain.

However, the reference of Miller does teach signals L0 to L7, which are the 8 bits of the DELAY SELECT control signal. These bits determine the length of the delay line by short circuiting or bypassing shift registers. (See fig. 3 & col. 5, lines 52-60)

Therefore, it would have been obvious to one of ordinary skills in the art to

incorporate this feature into the system of Miller, in the manner as claimed, for the benefit of determining and reducing the length of the delay line.

9. **Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434)**

Re claim 17, the reference of Miller fails to explicitly teach performed in response to receiving a signal of completion of a processing event.

However, the reference of Miller does suggest the teaching of mode control which, in response to determining a clock select, determines the speed with which the signal moves through the delay line. (See fig. 1: 26 "CLOCK SELECT" & col. 1, lines 54-56 & col. 4, lines 24-26)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed, for the benefit of selecting the rate which samples are shifted through the delay line.

10. **Claims (19-20) are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (hereinafter Miller) (US Patent 4,368,434)**

Re claim 19, the reference of Miller fails to explicitly teach wherein the processor is a state- machine.

However, the reference of Miller does teach signals L0 to L7, which are the 8 bits of the DELAY SELECT control signal. These bits determine the length of the delay line by short circuiting or bypassing shift registers. (See fig. 3 & col. 5, lines 52-60)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Miller, in the manner as claimed, for the benefit of determining and reducing the length of the delay line.

Claim 20 has been analyzed and rejected w/r to claim 19 above.

Claims (1, 14-15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren et al. (hereinafter Warren) (US Patent 6,075,807)

Re claim 1, Warren discloses a method of digitally processing a sequence of data samples comprising: reading the sequence of data samples into a tapped clocked delay chain (See fig. 1 & col. 3, lines 42-54); processing data samples from taps on the clocked delay chain. (See fig. 1 & col. 3, lines 42-54)

But the reference of Miller fails to explicitly teach that in response to receiving a signal of completion of a processing event, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain.

However, the reference of Warren does suggest that (See fig. 1 & col. 4, lines 33-37) in response to receiving a signal of completion of a processing event ("after synchronization has been achieved"), shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain. ("adjust the propagation rate of the delay line")

Therefore, it would have been obvious (obvious to try) to one of ordinary skills in

the art to incorporate this feature into the system of Warren, in the manner as claimed, for the benefit of adjusting the rate which samples are shifted through the delay line.

The reference of Warren discloses the limitations as claimed above, except he fails to explicitly teach dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain.

However, the reference of Warren does suggest (See fig. 1 & col. 4, lines 33-37) dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain. ("adjust the propagation rate of the delay line")

Therefore, it would have been obvious (obvious to try) to one of ordinary skills in the art to incorporate this feature into the system of Warren, in the manner as claimed, for the benefit of determining and reducing the length of the delay line.

Claim 14 is an apparatus claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in apparatus claim 14. Therefore, claim 14 has been analyzed w/r to claim 1 above.

Claim 15 has been analyzed and rejected w/r to claim 1 above.

Claims (1, 14-15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (hereinafter "Prior art") in view of Alexander. (US Patent 6,765,419 B2)

Re claim 1, Prior art discloses a method of digitally processing a sequence of

data samples comprising: reading the sequence of data samples into a tapped clocked delay chain (See Background of invention, page 2 lines 6-11); processing data samples from taps on the clocked delay chain. (See Background of invention, page 2 lines 6-11)

But the reference of Prior art fails to explicitly teach that in response to receiving a signal of completion of a processing event, shifting data samples rapidly out of the clocked delay chain at a higher output rate than an input rate of data samples coming into the clocked delay chain; and dynamically reducing the length of the clocked delay chain as data samples continue to be read into the clocked delay chain.

However, Alexander does. (See figs 1-3 & col. 2, lines 15-22, col. 4, lines 16-25) Alexander discloses a method of reducing the length of a delay line in response to a control signal.

Therefore, taking the combined teachings of Prior art and Alexander as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Prior art, in the manner as claimed and as taught by Alexander, for the benefit of reducing the length of the delay chain.

Claim 14 is an apparatus claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in apparatus claim 14. Therefore, claim 14 has been analyzed w/r to claim 1 above.

Claim 15 has been analyzed and rejected w/r to claim 1 above.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. F./
Examiner, Art Unit 2611
October 9, 2008

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611